Amendments to the Claims

1. (*Currently Amended*) Method of forming a semiconductor device having a gate, comprising:

[[-]]providing a first layer ~~(6)~~ of amorphous gate material,

[[-]]doping ~~(8)~~ the first layer ~~(6)~~ of amorphous gate material, thus forming a doped first layer of amorphous gate material,

[[-]]thermally activating the doped first layer of gate material, thus forming an activated first layer of gate material ~~(10)~~, and

[[-]]providing a second layer ~~(16)~~ of gate material on top of the activated first layer of gate material ~~(10)~~.

2. (*Currently Amended*) A method according to claim 1, wherein the first and second layers of gate material ~~(6, 10)~~ are silicon-based.

3. (*Currently Amended*) A method according to claim 1, further comprising patterning the second layer ~~(16)~~ of gate material and the activated first layer of gate material ~~(10)~~ to form one or more gates on the substrate ~~(2)~~.

4. (*Currently Amended*) A method according to claim 1, wherein providing a first layer ~~(6)~~ of amorphous gate material includes forming a layer of amorphous gate material having a thickness of about 10 nm to about 40 nm. ~~having a thickness of about 10 nm to 40 nm, preferably about 20 nm to 30 nm.~~

5. (*Currently Amended*) A method according to claim 1, wherein providing a second layer (16) of gate material includes forming a layer of gate material having a thickness of about 50 nm to about 150nm. ~~having a thickness of about 50 nm to 150 nm, preferably about 70 nm to 130 nm.~~

6. (*Currently Amended*) An MIS type semiconductor device, comprising:

[[-]]a semiconductor substrate ~~(2)~~,

[[-]]a gate electrode formed on the gate insulating film and formed of gate material,

wherein the gate electrode comprises:

[[-]]a first layer ~~(10)~~ of activated crystalline gate material having a first side oriented towards a substrate ~~(2)~~ and a second side oriented away from the substrate ~~(2)~~, the first layer ~~(10)~~ of activated crystalline gate material having a doping level of 10^{19} ions/cm^3 or higher, and

[[-]]a second layer ~~(16)~~ of gate material at the second side of the first layer ~~(10)~~ of activated crystalline gate material.

7. (*Currently Amended*) A semiconductor device according to claim 6, wherein the first layer ~~(10)~~ of activated crystalline gate material has a doping level of about 10^{20} ions/cm^3 or higher. ~~or higher, preferably $5x10^{20}$ ions/cm3 or higher.~~

8. (*Currently Amended*) An MIS type semiconductor device according to claim 6, wherein the doping implant in the activated gate material has an abruptness of about 2 nm or more. ~~an abruptness of 2 nm or more, preferably 1.5 nm or more, most preferred about 1 nm.~~

9. (*Currently Amended*) A semiconductor device according to claim 6, wherein the second layer ~~(16)~~ of gate material consists of amorphous gate material.

10. (*Currently Amended*) A semiconductor device according to claim 6, wherein the second layer ~~(16)~~ of gate material consists of polycrystalline gate material.

11. (*Currently Amended*) A semiconductor device according to claim 6, wherein the grain size in the second layer is below about 40 nm. ~~below 40 nm, preferably below 30 nm.~~

12. (*Original*) A semiconductor device according to claim 6, wherein the first layer is crystalline or very fine-grained, with grains below 5 nm.

13. (*Currently Amended*) A semiconductor device according to claim 6, wherein a gate insulator ~~(4)~~ is provided between the semiconductor substrate ~~(2)~~ and the gate electrode.

14. (*Original*) A semiconductor device according to claim 6, wherein the device is a transistor.

15. (*New*) A method according to claim 1, wherein providing a first layer of amorphous gate material includes forming a layer of amorphous gate material having a thickness of about 20 nm to 30 nm.

16. (*New*) A method according to claim 1, wherein providing a second layer of gate material includes forming a layer of gate material having a thickness of about 70 nm to about 130 nm.

17. (*New*) A semiconductor device according to claim 6, wherein the first layer of activated crystalline gate material has a doping level of about 5×10^{20} ions/cm^3 or higher.

18. (*New*) An MIS type semiconductor device according to claim 6, wherein the doping implant in the activated gate material has an abruptness of about 1.5 nm or more.

19. (*New*) An MIS type semiconductor device according to claim 6, wherein the doping implant in the activated gate material has an abruptness of about 1 nm.

20. (*New*) A semiconductor device according to claim 6, wherein the grain size in the second layer is below about 30 nm.